Improvement of Address Discharge Characteristics Using Asymmetric Variable-Width Scan Waveform in ac Plasma Display Panel

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***Abstract*—A new asymmetric variable-width scan waveform is proposed to improve the characteristics of an address discharge, including a reduced address time and increased dynamic voltage margin, based on the formative and statistical time lags of an address discharge in an ac-plasma display panel (ac-PDP). The new asymmetric variable-width scan waveform has a progressively increasing scan pulsewidth that is wider than the address pulsewidth, thereby enabling stable wall charge accumulation under short address pulsewidth conditions. When adopting this new scan waveform, the address pulsewidth was reduced from 3.0 to 1.4 μs and the address voltage lowered from 65 to 55 V without any misfiring problem at an address pulsewidth of 1.4 μs.**

***Index Terms*—Address discharge characteristics, asymmetric variable-width scan waveform, dynamic voltage margin, plasma display panel.**

I. Introduction

THE address-display-separated (ADS) driving method is considered to be the most suitable driving technique for an ac-plasma display panel (ac-PDP) [1], [2]. However, the ADS driving method has to reduce a long address time for the successful realization of a high-definition PDP with extended graphics array (XGA) resolution. It is well-known that the address discharge strongly depends on the reset discharge due to the priming effect [3]. The space charges remaining in the PDP cell after a reset discharge affect the ensuing address discharge as priming particles during an address period. These priming particles contribute to improving the discharge characteristics. However, since the address procedure is carried out line by line after the reset discharge, the priming particles continuously decrease during a long address period, thereby inducing the formative and statistical time lags of the address discharge [4]–[6]. On the other hand, other types of the priming particles for address discharge in a certain cell are also delivered by address discharge of adjacent cells [7]. Unlike the priming particles delivered by the reset discharge, these priming particles from adjacent cells play a role in deteriorating the address discharge characteristics by removing the part of the wall charges accumulated on the address electrodes by the previous reset discharge. The loss of the wall charges due to the transport of the electrons produced by the address discharge of adjacent cell also causes the formative and statistical time lags, thereby resulting in the increase in the address voltage [7]. Nonetheless, the discharge time lag phenomenon caused by the neighboring address discharge is excluded in the current paper because this problem strongly depends on the cell geometry [7], indicating that the formative and statistical time lags due to the neighboring address discharge can be reduced considerably if the barrier ribs with closed shape such as the waffle [8] or segmented electrode in delta color arrayed rectangular subpixels (SDR) [9] structure are adopted instead of the open shape such as a stripe type.

In general, the formative and statistical time lags of the address discharge can be reduced if the address voltage is increased [10]. However, the priming particles delivered by the reset discharge decrease with time. As such, the application of a higher address voltage during an address period would give rise to a misfiring discharge in cells with many priming particles, while an address discharge would still be efficiently produced in cells with few priming particles. On the other hand, a low address voltage would be unable to produce an address discharge efficiently in cells with few priming particles, even though no misfiring discharge is produced in cells with many priming particles due to the low address voltage. Accordingly, the improvement of the address discharge including a short address time and low address voltage appears to be very difficult, because the priming particles delivered by the previous reset discharge vary with a line-by-line address scanning procedure [10]. To solve this problem, many research results on address discharge characteristics have been reported [10]–[13]. In particular, it has been stated that the address time can be reduced from 3.0 to 2.1 μs by utilizing different address voltages progressively increased from 70 to 80 V as the address pulses [10]. However, this method causes an increase in the address voltage, resulting in a narrow dynamic voltage margin. In addition, the difficulty of providing a linearly increasing voltage for the address voltage results in a high-driving cost.

In the current paper, the formative and statistical time lags of the address discharge are measured at different scan pulsewidths of 3.0 and 1.4 μs. In addition, the dynamic voltage margin is also checked relative to a variation in the scan pulsewidth from 3.0 to 1.4 μs. Based on the formative and statistical time lags of an address discharge induced by the reset discharge, a new asymmetric variable-width scan waveform is proposed to simultaneously reduce the address time and increase the dynamic voltage margin. The main idea of the proposed asymmetric scan method

Manuscript received November 19, 2002; revised March 4, 2003. This work was supported by the Brain Korea 21 Project in 2002. The review of this paper was arranged by Editor J. Hynecek.

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Digital Object Identifier 10.1109/TED.2003.813452

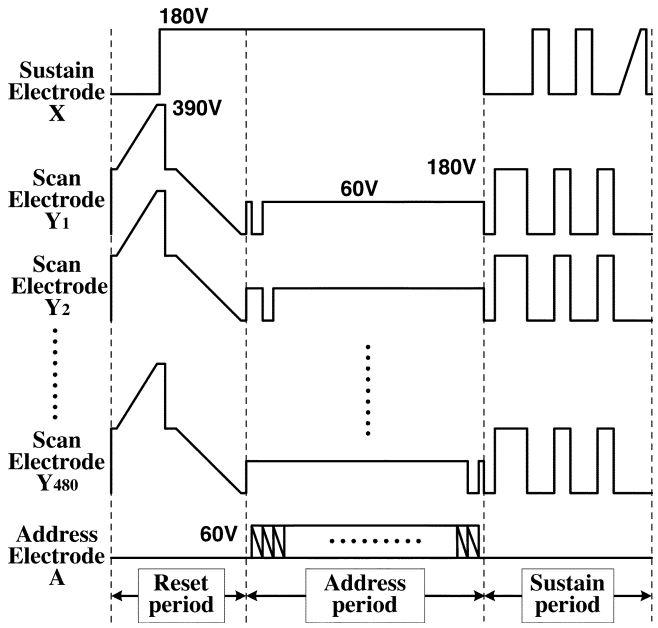

Fig. 1. Conventional driving waveforms for reset, address, and sustain periods in case of VGA degree PDP panel with 480 scan lines.

is to widen the scan pulsewidth under short address pulse condition because a scan pulse wider than the address pulse can compensate an insufficient accumulation of the wall charges for the next stable sustain discharge. If a misfiring problem is not considered, it is expected that the wider the scan pulsewidth, the better the address characteristics under short address pulse condition. Accordingly, in the case of the asymmetric variable-width scan waveform, the time intervals for the variable width of the scan pulse wider than the address pulse are precisely determined by considering the variations in the formative time lags of the address discharge due to the disappearance of the priming particles with time.

II. Experiment

A. Formative and Statistical Time Lags of Address Discharge Induced by Reset Discharge in a Conventional Symmetric Scan Method

Fig. 1 shows the conventional driving waveforms for the reset, address, and sustain periods in the case of a video graphics array (VGA) degree PDP with 480 scan lines. For the address procedure after the reset procedure in Fig. 1, scan and address pulses are successively applied between the scan and address electrodes, Y and A, from the scan line Y_1 to Y_{480}. In the conventional symmetric scan method, the scan pulsewidth is equal to the address pulsewidth. Since the address procedure is carried out line by line immediately after the reset procedure, the address discharge characteristics, such as the discharge formative and statistical time lags, vary depending on the time interval between the reset and address discharges [14]. Accordingly, a sufficient scan time for each scan line is required to produce a stable address discharge for all the scan lines. The conventional scan pulsewidth (or address pulsewidth) is about 3 μs.

Fig. 2(a) illustrates the electric circuit diagram of the 4-in test panel employed in the current study. The specifications of

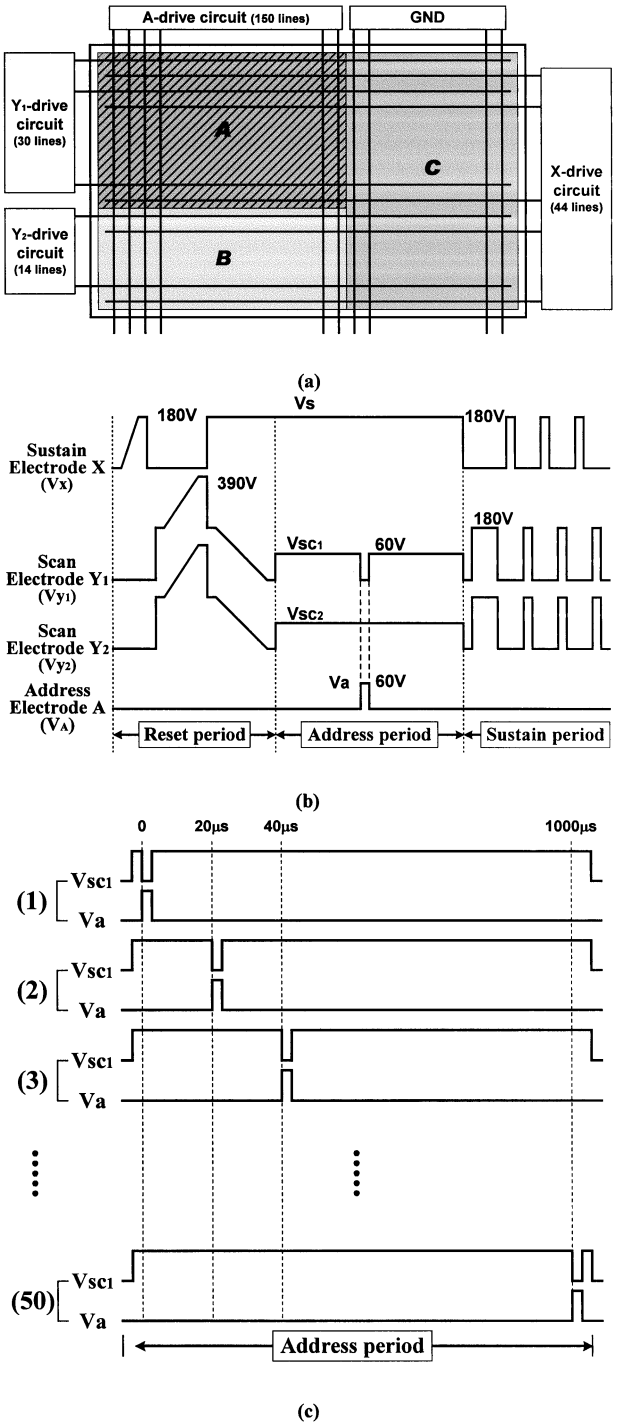

Fig. 2. Electric circuit diagram of (a) 4-in ac-PDP test panel and (b) driving waveforms with scanning waveforms for (c) address discharge employed in the current study. (a) Test panel with 44 scan lines is separated into three regions (A: address discharge region, B: misfiring checking region between Y and A, C: misfiring checking region between X and Y). (b) Driving waveforms for reset, address, and sustain periods applied to three electrodes X, Y, and A. (c) Scan and address pulses, V_{y1} and V_a, applied between scan and address electrodes Y_1 and A, during address period.

the test panel are listed in Table I. The gas used was a He–Ne (7 : 3)–Xe(4%) mixture, at a pressure of 400 torr. The driving conditions were a sustain voltage of 180 V, sustain frequency of 125 kHz, and sustain pulsewidth of 3.0 μs. To determine the dynamic voltage margin with respect to the various scan driving

TABLE I
SPECIFICATIONS OF 4-IN ac-PDP TEST PANEL EMPLOYED IN CURRENT STUDY

Front panel		Rear panel	
ITO width	310 μm	Address electrode width	100 μm
ITO gap	60 μm	Barrier rib height	130 μm
Bus width	100 μm	Barrier rib pitch	420 μm
Dielectric thickness	30 μm	Barrier rib width	80 μm

methods, the 4-in test panel was divided into three regions A, B, and C, as shown in Fig. 2(a). In region A, an address discharge was produced to investigate the effects of the new scan waveform, whereas the corresponding misfiring discharge between the scan and address electrodes, Y and A, was checked in region B. The misfiring discharge between the sustain and scan electrodes, X and Y, was also checked in region C. Fig. 2(b) shows the driving waveforms for the reset, address, and sustain periods applied to the three electrodes X, Y, and A in the 4-in test panel employed in the current study. As shown in Fig. 2(b), the pulses V_{x} for the reset, address, and sustain periods were commonly applied to all the sustain electrodes X with 44 lines through the X-drive circuit. The pulses V_{y1} and V_{y2} applied to the scan electrodes Y_1 and Y_2 through the Y_1- and Y_2-driver circuits were the same for the reset and sustain periods, yet not for the address period. In particular, V_{s} means the sustain pulse applied to the sustain electrode X during an address period, whereas V_{sc} and V_{a} mean the scan and address pulses applied to the scan and address electrodes Y and A during an address period, respectively. For the address procedure, scan pulses V_{sc1} of 60 V and address pulses V_{a} of 60 V were simultaneously applied to only the 30 scan lines and the 150 address lines in region A through the Y_1- and A-drive circuits, as shown in the address period in Fig. 2(b). Fig. 2(c) illustrates the scan and address pulses V_{s1} and V_{a} applied to the scan and address electrodes, Y_1 and A, respectively, in region A during an address period. To investigate the formative and statistical time lags of the address discharge, as shown in Fig. 2(c), the scan and address pulses V_{s1} and V_{a} were applied at time intervals of 20 μs from 0 to 1000 μs after applying the reset pulses in Fig. 2(b). In particular, the widths of the address and scan pulses were varied from 1.4 to 3.0 μs so as to observe any changes in the formative and statistical time lags of the address discharge with a variation in the pulsewidth.

Fig. 3 shows the formative and statistical time lags of the address discharge when address and scan pulses with different widths [(a): 3.0 μs and (b): 1.4 μs] were applied at time intervals of 20 μs from 0 to 1000 μs after the reset discharge during an address period. The formative and statistical time lags of Fig. 3(a) and (b) were measured from the IR (823 nm) waveform for 36 cells in region A when the scan and address pulses were applied to the 4-in test panel of Fig. 2(a) during an address period. Fig. 4(a) shows the formative and statistical time lags defined form the IR (823 nm) waveform emitted from the address discharge produced by applying the scan and address pulses during an address period. Fig. 4(b) shows the changes in the formative and statistical time lags with variations in the time intervals of 20 μs from 0 to 1000 μs after the reset discharge when address and scan pulses with different widths were applied during an address period. While carrying out the scanning procedure, i.e.,

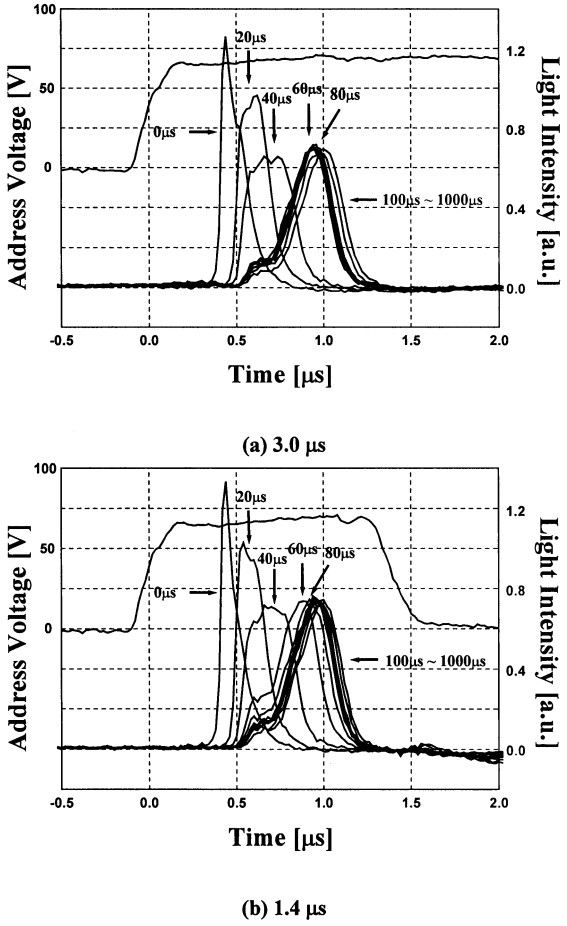

Fig. 3. Address discharge characteristics with variation in scanning time from 0 to 1000 μs at different scan pulsewidths of: (a) 3 μs and (b) 1.4 μs.

increasing the scanning time based on line-by-line scanning, the discharge formative and statistical time lags were protracted, as shown in Figs. 3 and 4, indicating that the priming effect was decreased with the scanning procedure. In particular, it was observed that the formative time lags of the address discharge were nearly saturated when the scan pulses were applied after 80 μs from the reset discharge, implying that the priming effect only existed for 80 μs during the total scanning procedure, regardless of the different pulsewidths. The tendency exhibited by the formative and statistical time lags of the address discharge were similar irrespective of a difference in the scan pulsewidth, as shown in the measurement results in Fig. 4. This result shows that the formative and statistical time lags of the address discharge do not depend on the scan pulsewidth but rather on the priming effect caused by the previous reset discharge.

Fig. 5 illustrates the changes in the dynamic voltage margin regions at different scan pulsewidths of: (a) 3.0 μs, (b) 2.0 μs, and (c) 1.4 μs during an address period of 1000 μs when using the conventional symmetric scan method. The formative and statistical time lags of the address discharge exhibited a similar tendency irrespective of differences in the scan pulsewidth, as indicated in Fig. 4. Nonetheless, the dynamic voltage margin was significantly affected by a difference in the scan pulsewidth, which implies that a wide scan pulsewidth is required to accumulate a large amount of wall charges for a stable sustain dis-

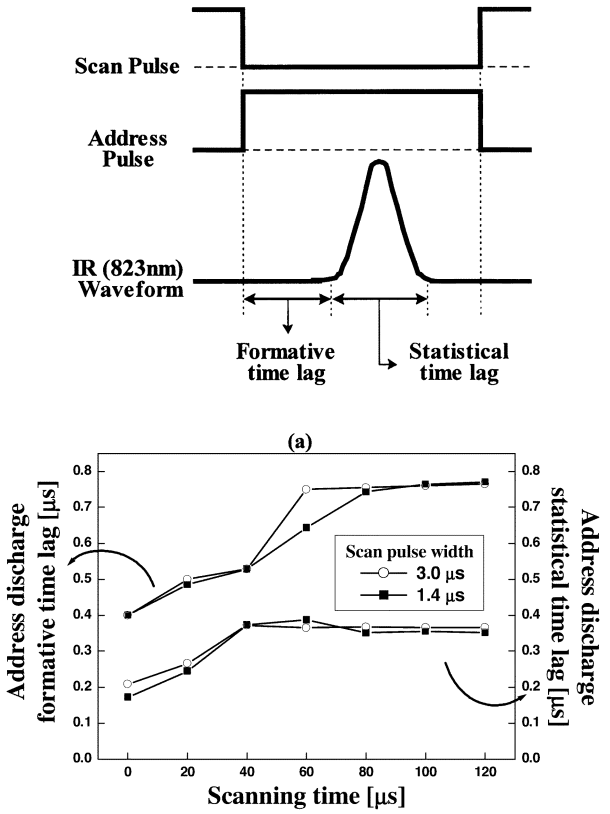

Fig. 4. Formative and statistical time lags of address discharge with variation in scanning time at different scan pulsewidths of 3 and 1.4 μs.

charge. Consequently, in the case of the narrow scan pulsewidth shown in Fig. 5, the dynamic voltage margin was significantly reduced due to insufficient time for a stable wall charge accumulation. In the current study, when the scan pulsewidth was 1.4 μs, a high address voltage above 65 V was required for a stable sustain discharge, as shown in Fig. 5. Consequently, for the conventional symmetric scan method, the scan pulsewidth must be determined based on a stable wall charge accumulation for the subsequent sustain discharge and the formative and statistical time lags of the address discharge.

B. Proposed Asymmetric Scan Method Based on Formative and Statistical Time Lags of Address Discharge

The two cells, 1 and 2, as shown in Fig. 6(a), are used to explain the basic principle of an asymmetric scan method and discuss the related misfiring problem. When the address procedure is carried out using an asymmetric scan method, cell 1 is selected to display an image, i.e., cell 1 is an on-cell that produces an address discharge, whereas cell 2 is chosen not to display an image, i.e., cell 2 is an off-cell where no address discharge is produced. Fig. 6(b) illustrates the sustain, scan, and address waveforms, $V_{\rm s}$, $V_{\rm sc}$, and $V_{\rm a}$, applied to the two cells 1 and 2 in Fig. 6(a), and also shows the corresponding IR emission waveforms for the two cells 1 and 2. Fig. 6(c) and (d) shows the corresponding temporal behavior model of the wall/space charges within the two cells, 1 and 2, respectively. Wall charges were accumulated on the three electrodes X, Y, and A_1 in cell 1 after the reset discharge, as shown in ① of cell 1 in Fig. 6(c) [15]. Yet, when the voltage level of scan

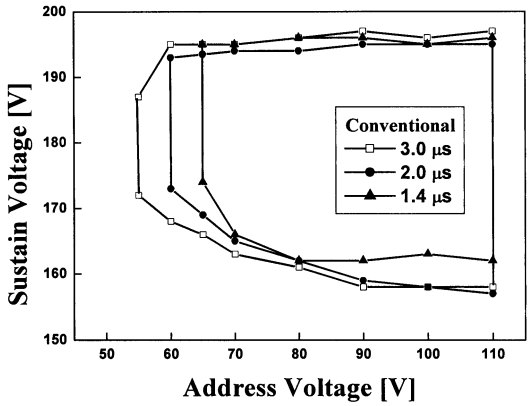

Fig. 5. Dynamic voltage margin relative to different scan pulsewidths of 3, 2, and 1.4 μs when adopting conventional symmetric scan driving method.

pulse $V_{\rm sc}$ fell abruptly from 60 to 0 V, while the voltage level of address pulse $V_{\rm a}$ simultaneously increased rapidly from 0 to 60 V, the firing of an address discharge was delayed, as shown in the IR emission of Fig. 6(b), indicating the existence of a certain time interval between ② and ③ in Fig. 6(b). This formative time lag of an address discharge varied according to the variation in the reset discharge state. As shown in ③ of cell 1 in Fig. 6(c), the wall charges began to accumulate on the electrodes X and Y immediately after an address discharge was produced. In the case of a short address or scan pulse (1.4 μs) with the conventional symmetric scan method, if the address voltage was not raised to a higher level, the amount of accumulated wall charges was insufficient because the address pulsewidth was too short to produce a stable wall charge accumulation for the subsequent sustain discharge.

To compensate for this problem, i.e., to accumulate more wall charges within 1.4 μs, the voltage level of the scan pulse $V_{\rm sc}$ was left at 0 V for a certain time interval Δt, even though the voltage level of address pulse $V_{\rm a}$ had already been lowered from 60 to 0 V. This is the new asymmetric scan waveform proposed in the current work, where the width of the scan pulse $V_{\rm sc}$ is wider than that of the address pulse $V_{\rm a}$. In this case, a high electric field intensity between the sustain and scan electrodes, X and Y, was maintained for a longer time because the voltage level of scan pulse $V_{\rm sc}$ remained at zero. As a result, the high electric field intensity helped to accumulate more wall charges on the sustain and scan electrodes, X and Y, even though the address pulse $V_{\rm a}$ was short. Accordingly, based on the new asymmetric scan waveform, the short address pulse $V_{\rm a}$ contributed to a reduction in the scanning time necessary for the scan electrode Y, meanwhile, the wider scan pulse $V_{\rm sc}$ contributed to a stable wall charge accumulation between the sustain and scan electrodes, X and Y.

However, the misfiring discharge caused by the wider scan pulse $V_{\rm sc}$ in cell 2 needs to be examined carefully. As shown in ② and ③ of cell 2 in Fig. 6(d), the wall charges accumulated on the three electrodes X, Y, and A_2 remained almost unchanged because the address voltage applied to the address electrode A_2 remained at zero in the case of lowering the voltage level of scan pulse $V_{\rm sc}$ from 60 to 0 V to produce an address discharge in cell 1. There was no discharge in cell 2 even though the voltage difference between $V_{\rm s}$ and $V_{\rm sc}$ was 180 V, as shown in

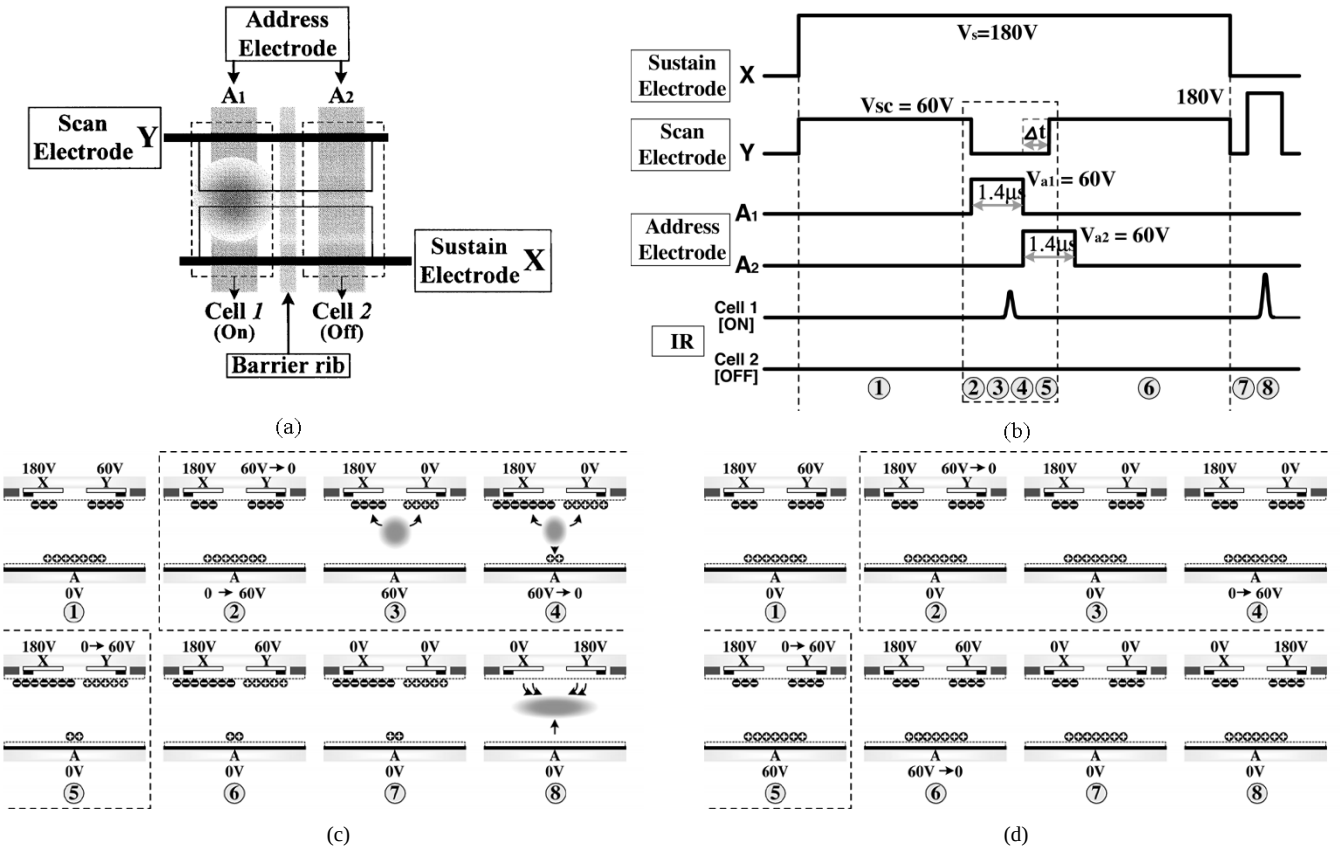

Fig. 6. Cells 1 and 2. (a) Selected arbitrarily in 4-in ac-PDP test panel for explaining and discussing principle of new asymmetric scan driving method and related misfiring problems where cell 1 is discharge-on cell and cell 2 is discharge-off cell. (b) Asymmetric scan and address waveforms, and IR (823 nm) waveforms. (c) Emitted from cells 1 and 2 with corresponding temporal behavior model of wall/space charges within cells 1 (c) and (d) 2.

the IR emission of cell 2 in Fig. 6(b). When another address pulse V_{a2} was applied to address electrode A_2 for addressing the next scan line, no misfiring discharge was observed to be produced in cell 2 on condition that the time interval Δt in the asymmetric part of the wider scan pulse $V_{\rm sc}$ was shorter than the address discharge formative time lag. In other words, as shown in ⑤ of cell 2 in Fig. 6(d), the electric field intensity among the three electrodes X, Y, and A_2 in cell 2 became weak when increasing the voltage level of scan pulse $V_{\rm sc}$ from 0 to 60 V before the address discharge firing, thereby prohibiting the undesirable misfiring discharge in cell 2. As a result, it is important to determine the proper time interval Δt for the asymmetric scan pulse $V_{\rm sc}$ in Fig. 6(b) to prevent a misfiring discharge. Hence, the time interval Δt in the asymmetric scan pulse $V_{\rm sc}$ in Fig. 6(b) should be varied according to the address discharge formative time lag caused by the priming effect of the reset discharge. As such, the proposed asymmetric scan method can be separated into two cases: one where the time interval Δt in the asymmetric scan pulse $V_{\rm sc}$ of Fig. 6(b) is constant, i.e., the width of the wider scan pulse $V_{\rm sc}$ remains constant, irrespective of the scan lines, and the other where the time interval Δt in the asymmetric scan pulse $V_{\rm sc}$ of Fig. 6(b) is variant, i.e., the width of the wider scan pulse $V_{\rm sc}$ is varied depending on the scan lines. In this experiment, the dynamic voltage margin with respect to the proposed asymmetric scan method was obtained by checking the misfiring discharge for the configuration of Fig. 6(a) in the following way: i.e., the sustain pulse $V_{\rm s}$ and scan pulse $V_{\rm sc}$ in Fig. 6(b) were applied to the sustain and scan electrodes X and Y_1 (30 lines) in regions A and C in Fig. 2(a), and, simultaneously, the address pulses V_{a1} and V_{a2}, shown in Fig. 6(b), were applied to the address electrodes in the neighboring cells between the regions A and C in Fig. 2(a).

III. Result and Discussion

Fig. 7 shows an asymmetric scan method: 1) with a constant Δt, namely an asymmetric constant-width scan method, where Δt was 0.4 μs and its corresponding dynamic voltage margin and 2) relative to the scanning time from 0 to 100 μs, where the scanning time was defined as a time taken until the beginning of the address discharge after the reset discharge. In this case, the address pulsewidth was 1.4 μs, whereas the scan pulsewidth was fixed at 1.8 μs. As shown in Fig. 7(b), the dynamic voltage margin remained almost constant until the scanning time increased from 0 to 60 μs. However, with an increase in the scanning time above 80 μs, the dynamic voltage margin was significantly reduced, thereby increasing the address voltage. Therefore, to improve the dynamic voltage margin characteristic above 80 μs, a new asymmetric scan method with a progressively increasing scan pulsewidth, namely an asymmetric variable-width scan method, was adopted, as shown in Fig. 8(a). In this experiment, based on considering the formative time lag of the addressing discharge in Fig. 4, three types of scan pulsewidths were chosen depending on the scanning time as follows: 1) scan pulsewidth of 1.8 μs

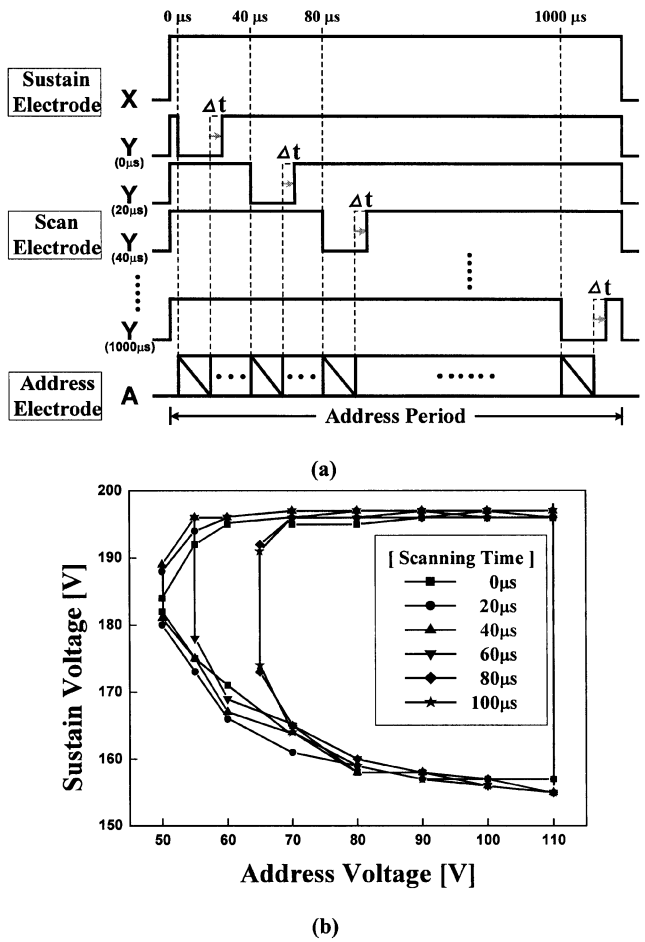

Fig. 7. (a) Asymmetric constant-width scan driving method and (b) corresponding dynamic voltage margin relative to scanning time.

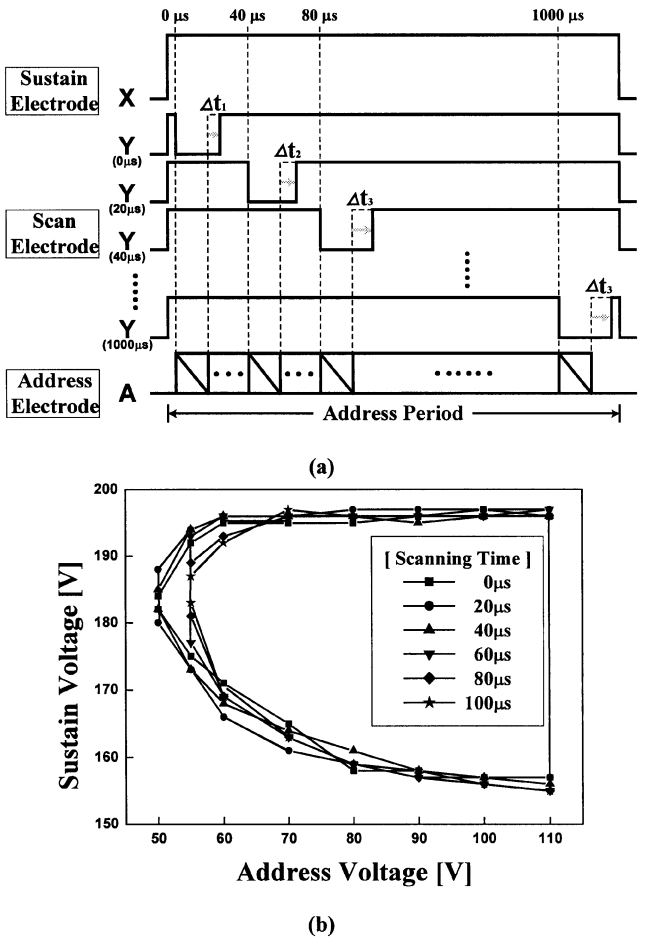

Fig. 8. (a) Asymmetric variable-width scan driving method and (b) corresponding dynamic voltage margin relative to scanning time.

($\Delta t_1 = 0.4$ μs) when scanning time ranged from 0 to 40 μs, 2) scan pulsewidth of 2.0 μs ($\Delta t_2 = 0.6$ μs) when scanning time ranged from 40 to 80 μs, and 3) scan pulsewidth of 2.2 μs ($\Delta t_3 = 0.8$ μs) when scanning time was above 80 μs. Because the discharge formative time lag was saturated above 80 μs, the scan pulsewidth for the scanning time above 80 μs was fixed at 2.2 μs. This increase of scan pulsewidth helped to accumulate more wall charges on the electrodes X and Y, resulting in a wide stable dynamic voltage margin even for a scanning time above 80 μs, as shown in Fig. 8(b).

The variations in the dynamic voltage margin according to the three types of scanning methods are illustrated in Fig. 9. The margin data in Fig. 9 shows that the new asymmetric variable-width scan method significantly improved the dynamic voltage margin characteristic, when compared with the conventional symmetric method or asymmetric constant-width scan method. As indicated by the result for the asymmetric variable-width scan method of Fig. 9, the voltage level of address pulse was reduced to 55 V with an address pulsewidth of 1.4 μs.

Fig. 10 shows the changes in the IR intensity when a first sustain voltage of 180 V was applied with a variation in the scanning time at time intervals of 20 μs from 0 to 100 μs after the address discharge to examine whether or not sufficient wall charges were accumulated in the case of adopting the three

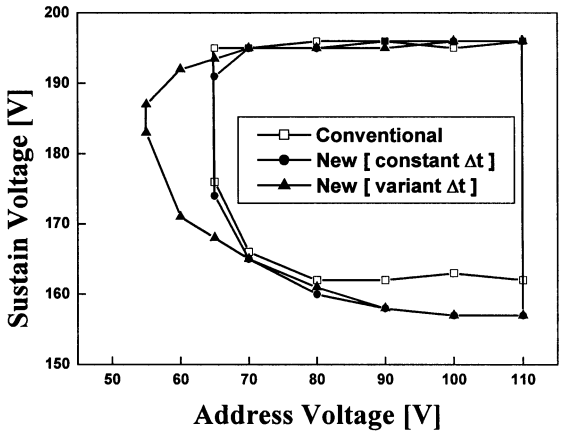

Fig. 9. Dynamic voltage margin relative to three types of scanning methods. Conventional symmetric scan method, asymmetric constant-width scan method, and asymmetric variable-width scan method.

types of scanning methods with an address pulsewidth of 1.4 μs [(a) conventional symmetric scan method, (b) asymmetric constant-width scan method, and (c) asymmetric variable-width scan method]. As shown in Fig. 10, the IR emission characteristics of the first sustain discharge were the best when adopting the new asymmetric variable-width scan method.

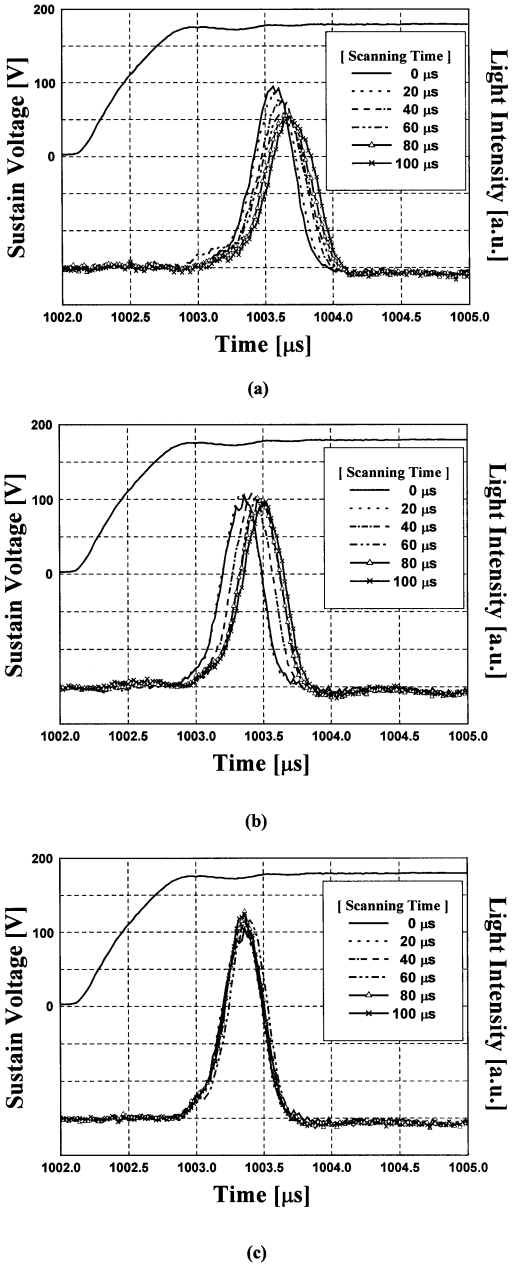

Fig. 10. Changes in IR intensity when first sustain voltage is applied with variation in scanning time at time intervals of 20 μs from 0 to 100 μs after address discharge. (a) Conventional symmetric scan method. (b) Asymmetric constant-width scan method. (c) Asymmetric variable-width scan method.

IV. Conclusion

This paper proposes a new asymmetric scan method for improving the characteristics of an address discharge, including a reduced address time and increased dynamic voltage margin, based on its formative and statistical time lags. As a result of comparing three types of scanning methods, the conventional symmetric scan method, new asymmetric constant-width scan method, and new asymmetric variable-width scan method at an address pulsewidth of 1.4 μs, the asymmetric variable-width scan method exhibited the best address discharge characteristics, including a low address voltage of 55 V with a short address time of 1.4 μs and no misfiring problem.

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